100Gbps SR4 100m MPO QSFP28 Transceiver
PQ21H-8501M

Features

- ✓ Supports 103.1Gbps aggregate bit rates
- ✓ 4x25.78Gbps 850nm VCSEL transmitter and PIN receiver
- ✓ Maximum link length of 70m on OM3 MMF and 100m on OM4 MMF
- ✓ Single MPO receptacle
- ✓ Hot pluggable QSFP28 form factor
- ✓ Power dissipation < 2.5W
- ✓ All-metal housing for superior EMI performance
- ✓ RoHS6 compliant (lead free)
- ✓ Operating case temperature:
  Commercial: 0ºC to +70°C

Applications

- ✓ 100GBASE-SR4
- ✓ InfiniBand FDR/EDR

Standards

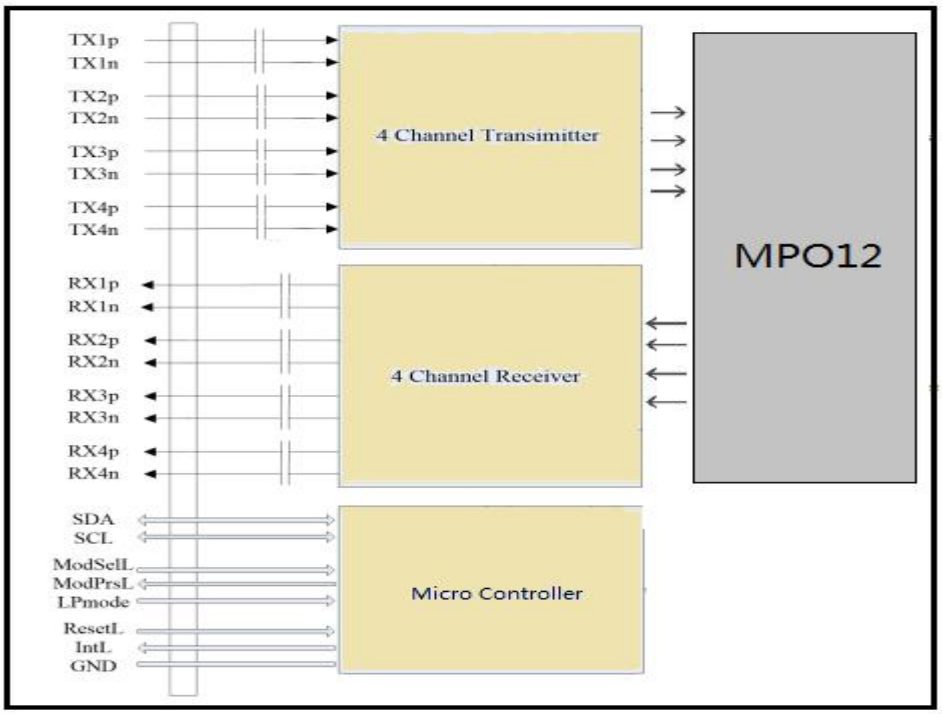
- ✓ Compliant with QSFP28 MSA
- ✓ Compliant with SFF-8636
- ✓ Compatible with IEEE802.3bm

Description

The QSFP28 transceivers are designed for use in 100-Gigabit Ethernet links up to 100m over Multimode Mode Fiber.

The transceivers are compatible with QSFP28 MSA and SFF-8636. For further information, please refer to QSFP28 MSA and SFF-8636.

Module Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit
Power Supply Voltage	V_{CC}	0		3.6	V
Storage Temperature	Ts	-40		+85	°C
Relative Humidity	RH	0		85	%
RX Input Average Power per Lane	P_{max}	-		3.5	dBm

Recommended Operating Environment

Parameter	Symbol	Min.	Typical	Max.	Unit
Power Supply Voltage	V_{CC}	3.13	3.3	3.46	V
Power Supply Current	I_{CC}			750	mA
Power Dissipation	P_D			2.5	W
Operating Case Temperature	T_C	0		+70	°C
Aggregate Data Rate	-		103.125		Gbps
Bit Rate per Lane	BR		25.78125		Gbps

Electrical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Transmitter Section						
Input Differential Impedance	R_{in}	90	100	110	Ω	
Differential Data Input Swing	$V_{in\ PP}$	180		1000	mV	1
Receiver Section						
Differential Data Output Swing	$V_{out\ PP}$	300		850	mV	

Notes:

1. Connected directly to TX data input pins. AC coupling from pins into laser driver IC.

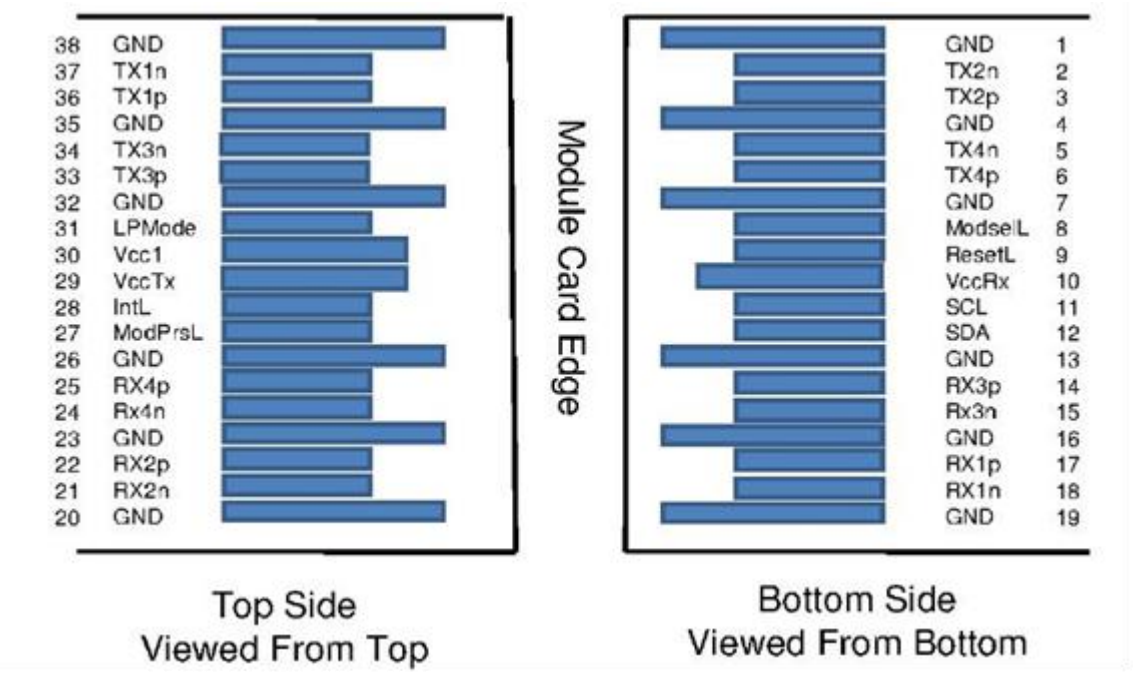
Optical Parameters

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Transmitter Section						
Lane Centre Wavelength (range)	λ_C	840		860	nm	
Spectral Width (RMS)	σ			0.6	nm	
Average Optical Power per Lane	P_{out}	-8.4		+2.4	dBm	1
OMA Power per Lane	OMA	-6.4		3	dBm	1
Laser Off Power per Lane	P_{off}	-	-	-30	dBm	
Extinction Ratio	ER	3	-	-	dB	2
Relative Intensity Noise	RIN	-	-	-128	dB/Hz	
Optical Return Loss Tolerance		-	-	12	dB	
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}	Compliant with IEEE802.3bm {0.3 0.38, 0.45, 0.35, 0.41, 0.5}					2
Receiver Section						
Lane Center Wavelength (range)	λ_C	840		860	nm	
Average Receiver Power per Lane	RXP_X	-10.3		2.4	dBm	3
OMA Stressed Sensitivity per Lane	RX_{sens}			-5.2	dBm	3
Los Assert	LOS_A	-30	-	-	dBm	
Los Dessert	LOS_D	-	-	-13	dBm	
Los Hysteresis	LOS_H	0.5	-	5	dB	
Overload per Lane	P_{in-max}	-	-	2.4	dBm	3
Receiver Reflectance		-	-	-12	dB	
Damage Threshold per Lane		-	-	3.5	dBm	

Notes:

1. The optical power is launched into 50/125μm MMF.
2. Measured with a PRBS 2^{31}-1 test pattern @25.78Gbps.
3. Measured with a PRBS 2^{31}-1 test pattern @25.78Gbps, ER=3dB, BER <10^{-12}.

Pin Definitions



Pin Descriptions

Pin	Symbol	Description	Plug Seq.	Notes
1	Ground	Ground	1	1
2	Tx2n	Transmitter Inverted Data Input	3	
3	Tx2p	Transmitter Non-Inverted Data Input	3	
4	Ground	Ground	1	1
5	Tx4n	Transmitter Inverted Data Input	3	
6	Tx4p	Transmitter Non-Inverted Data Input	3	
7	Ground	Ground	1	1
8	ModSelL	Module Select	3	
9	ResetL	Module Reset	3	
10	VccRx	+3.3 V Power supply receiver	2	2
11	SCL	2-wire serial interface clock	3	
12	SDA	2-wire serial interface data	3	
13	Ground	Ground	1	1
14	Rx3p	Transmitter Non-Inverted Data Input	3	
15	Rx3n	Transmitter Inverted Data Input	3	
16	Ground	Ground	1	1
17	Rx1p	Transmitter Non-Inverted Data Input	3	
18	Rx1n	Transmitter Inverted Data Input	3	
19	Ground	Ground	1	1
20	Ground	Ground	1	1

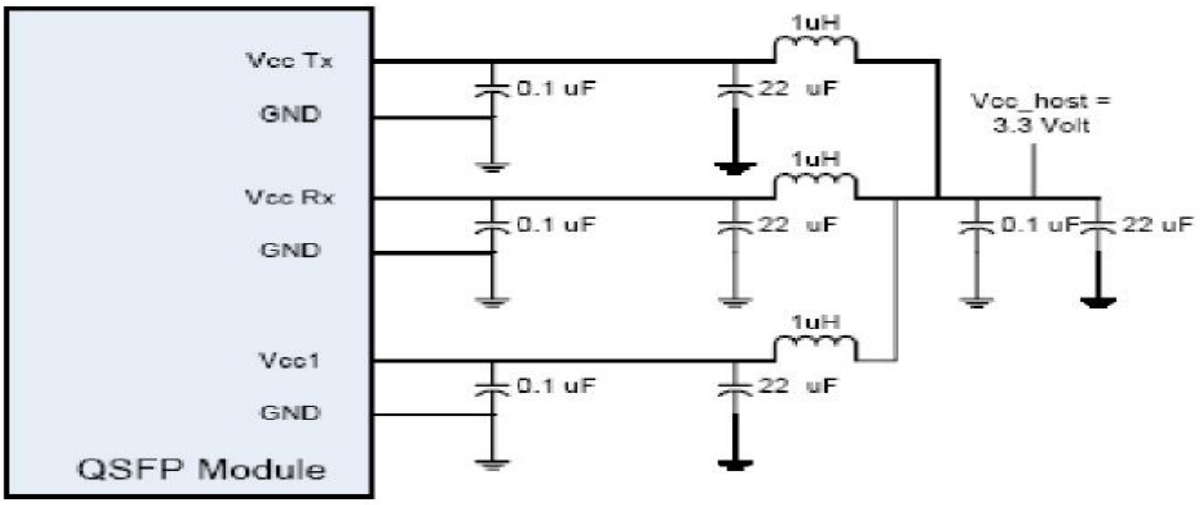
21	Rx2n	Transmitter Inverted Data Input	3	
22	Rx2p	Transmitter Non-Inverted Data Input	3	
23	Ground	Ground	1	1
24	Rx4n	Transmitter Inverted Data Input	3	
25	Rx4p	Transmitter Non-Inverted Data Input	3	
26	Ground	Ground	1	1
27	ModPrsL	Module Present	3	
28	IntL	Interrupt	3	
29	VccTx	+3.3 V Power supply transmitter	2	2
30	Vcc1	+3.3 V Power Supply	2	2
31	LPMode	Low Power Mode	3	
32	Ground	Ground	1	1
33	Tx3p	Transmitter Non-Inverted Data Input	3	
34	Tx3n	Transmitter Inverted Data Input	3	
35	Ground	Ground	1	1
36	Tx1p	Transmitter Non-Inverted Data Input	3	
37	Tx1n	Transmitter Inverted Data Input	3	
38	Ground	Ground	1	1

Notes:

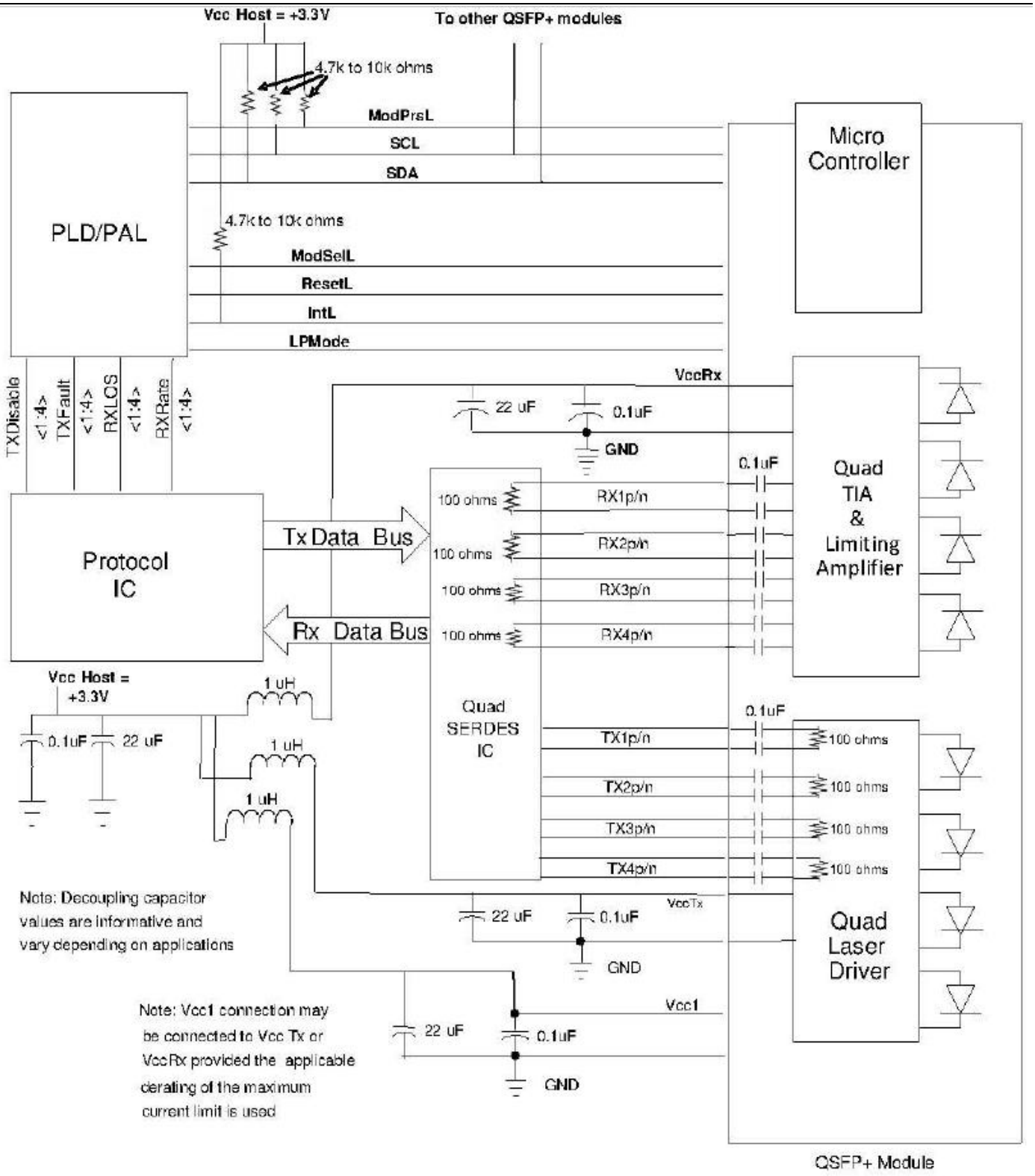
Plug Seq.: Pin engagement sequence during hot plugging.

1. Module ground pins GND are isolated from the module case.
2. VccRx, Vcc1 and VccTx are the receiver and transmitter power supplies and shall be applied concurrently.

Recommended Power Interface Circuit



Recommended Interface Circuit


Vcc Host = +3.3V
To other QSFP+ modules
4.7k to 10k ohms
ModPrsL
SCL
SDA
PLD/PAL
4.7k to 10k ohms
ModSelL
ResetL
IntL
LPMode
Micro Controller
TXDisable
<1:4>
TXFault
<1:4>
RXLOS
<1:4>
RXRate
<1:4>
VccRx
22 uF
0.1uF
GND
0.1uF
Quad TIA & Limiting Amplifier
100 ohms
RX1p/n
100 ohms
RX2p/n
100 ohms
RX3p/n
100 ohms
RX4p/n
Protocol IC
Tx Data Bus
Rx Data Bus
Vcc Host = +3.3V
1 uH
0.1uF
22 uF
1 uH
1 uH
Quad SERDES IC
0.1uF
TX1p/n
TX2p/n
TX3p/n
TX4p/n
100 ohms
100 ohms
100 ohms
100 ohms
VccTx
22 uF
0.1uF
GND
Quad Laser Driver
Note: Decoupling capacitor values are informative and vary depending on applications
Note: Vcc1 connection may be connected to Vcc Tx or VccRx provided the applicable derating of the maximum current limit is used
Vcc1
22 uF
0.1uF
GND
QSFP+ Module

Digital Diagnostic Functions

The QSFP28 transceivers support the 2-wire serial communication protocol as defined in the QSFP28 MSA, which allows real-time access to the following operating parameters:

- ✓ Transceiver temperature
- ✓ Laser bias current
- ✓ Transmitted optical power
- ✓ Received optical power
- ✓ Transceiver supply voltage

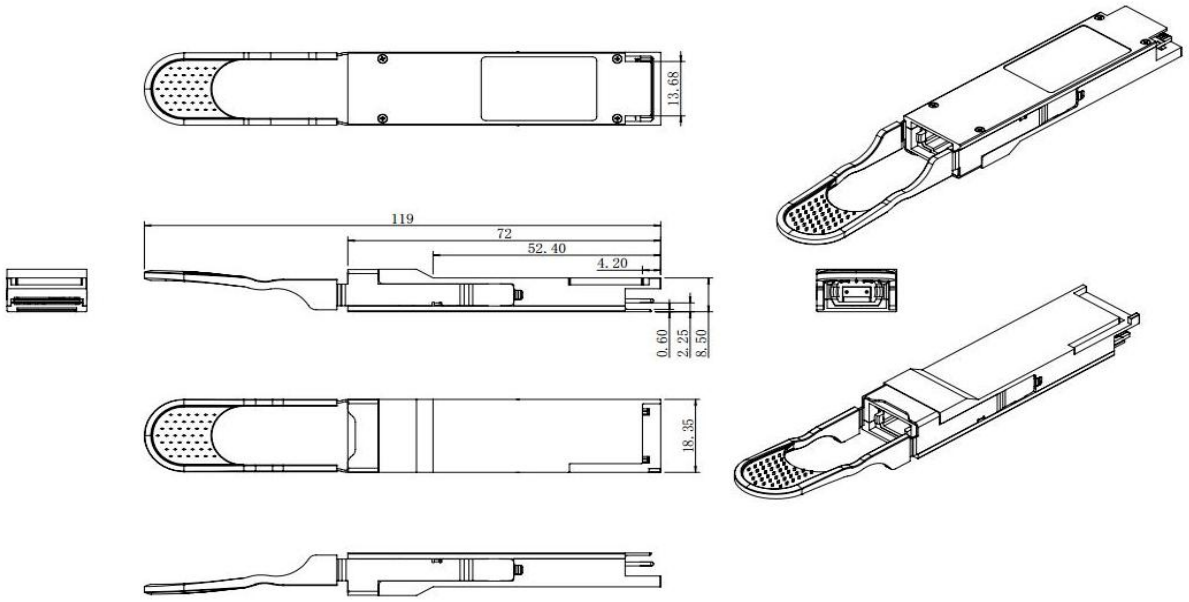
It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the QSFP28 transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the QSFP28 transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 00h to the maximum address of the memory.

This clause defines the Memory Map for QSFP28 transceiver used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all QSFP28 devices. The memory map has been changed in order to accommodate 4 optical channels and limit the required memory space. The structure of the memory is shown in Figure 2 QSFP28 Memory Map. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, e.g. Interrupt Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings, are available with the Page Select function. The structure also provides address expansion by adding additional upper pages as needed. For example, in Figure 2 upper pages 01 and 02 are optional. Upper page 01 allows implementation of Application Select Table, and upper page 02 provides user read/write space. The lower page and upper pages 00 and 03 are always implemented. The interface address used is A0 and is mainly used for time critical data like interrupt handling in order to enable a “one-time-read” for all data related to an interrupt situation. After an Interrupt, IntL, has been asserted, the host can read out the flag field to determine the effected channel and type of flag.

For more detailed information including memory map definitions, please see the QSFP28 MSA Specification.

Mechanical Dimensions



Ordering information

Part Number	Product Description
PQ21H-8501M	100Gbps QSFP28 SR4, 100m on MMF(OM4), MPO receptacle, 0ºC ~ +70ºC, With DDM.

References

1. SFF-8679 Specification for QSFP+ 4X Hardware and Electrical Specification.
2. SFF-8636 Specification for Management Interface for Cabled Environments.
3. IEE 802.3bm - PMD Type 100GBASE-SR4.

Important Notice

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Contact Information

PRIMUS IT LIMITED

1、HongKong：RM M4/F Continental Mansion 300 King's RD HK

2、Tel:+86 0755-25924025

3、Fax:+86 0755-25924051

4、Website：http://www.primus-it.com

5、Email：sales@primus-it.com